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Adiabatic Logic Gates using Wireless Charging

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Abstract

Adiabatic logic is the energy-efficient way of de- signing logic gates. The logic families like positive feedback adiabatic logic (PFAL), complementary pass-transistor logic (CPAL), and energy-efficient secure positive feedback adiabatic logic (EESPFAL) are used to design logic gates. The circuit using this logic has the potential in detecting hardware trojans (HT) using the power analysis method for detection. HT has become a major concern for the security of IoT devices. In recent times, the trend for wireless devices has increased and so has the threat. This motivates to development of wireless logic gates with low power consumption to secure the IoT devices. We propose a wireless powered adiabatic logic gate design. A practical wireless charging adiabatic circuit is demonstrated using LTSPICE simulation software. The circuit offers similar performance with the convenience of wireless connectivity.

Keywords: -Adiabatic logic; wireless power clock; CPAL; PFAL

Introduction

Since the last few decades, the amount of power consumption in the circuit has been a major cause of concern. There has been an immense demand for low power consumption devices. Though the conventional CMOS logic gate circuits provide low static power dissipation but during the switching operations the power dissipation increases. The adiabatic logic families like CPAL, PFAL are promising regarding the power consumption aspect [1] [2]. Eventually, the advancement in technology spurred the need for wireless connectivity for the internet of things (IoT) devices. A wireless adiabatic logic gate could be a potential solution to the demand.

Adiabatic Logic

Circuits made by using this logic consume comparatively less power than conventional CMOS circuits. The energy dissipation is given by:

$$E = \int I(t)^2 R \quad (1)$$

$$E = \frac{RC}{T} \int CV^2(t) \quad (2)$$

In Eq (2) when T >2RC then the energy dissipation is reduced [3]. In order to accomplish minimum energy dissipation, we employ a variable power supply that slowly ramps up to Vdd and then ramps down forming a trapezoidal waveform. This kind of power supply is provided by using a power clock in order to efficiently recycle the charge stored in the load capacitor. The waveform can be divided into four phases as shown in Fig 1: evaluate, hold, recovery and wait. During the evaluate phase the load capacitors are charged, inputs are observed and outputs are calculated. During the hold phase, the circuit holds the output. The recovery phase is the phase wherein the capacitor discharges and supplies the power back to the power clock. The circuit waits for further input during the wait phase. The charging and discharging of capacitors can be understood by Fig 2. This method reduces the dynamic switching energy loss in a circuit. The adiabatic family includes various members like CPAL, PFAL [4], EESPFAL [5] have been proposed for making logical and sequential circuits.

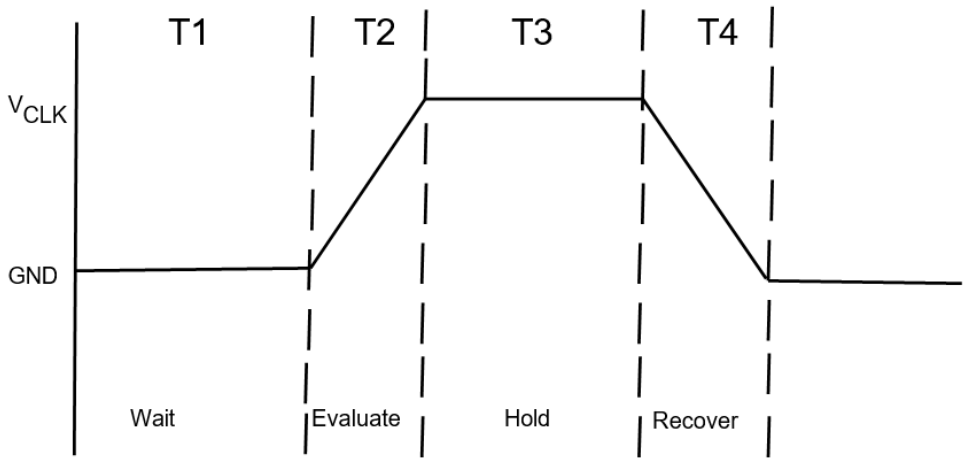

Fig.1.PowerClockdiagramanditphasesofworking

The wireless power transmission (WPT) is an approach to provide power to the receiver using a transmitter device, driven by a power source that generates a time-varying electro-magnetic field. Wireless power is generally transferred using electromagnetic fields which was first invented by Nikola Tesla in 1890 while experimenting with radio frequency resonant transformers. WPT has various approaches for power transmission out of which this paper uses the inductive power transfer (IPT). The circuit has two coils primary for transmission and secondary for a reception. The current through the primary coil induces an electric field in the secondary coil and so is the voltage supplied to the circuit wirelessly as the load end[6] [7].

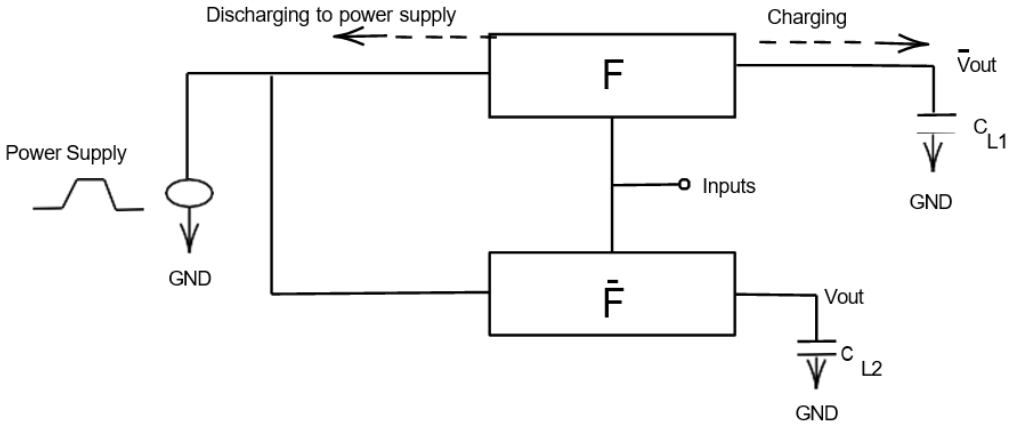

Fig.2.AdiabaticChargingandDischarging.

Previous Works

The concept of adiabatic logic is derived from thermodynamics which states that the heat dissipated to the environment through the system is zero. Using this concept, the adiabatic logic gates are designed which leads to a reduction in the heat energy losses. The working principle of adiabatic logic is the charging and discharging of the capacitor. One of the initial works was in 1997 by Vojin G. Oklobdzija et al was about pass transistor adiabatic logic (PAL) with a single-phase power clock that proved to be efficient in terms of energy and performance as compared to the previously proposed adiabatic families [8].

CPAL main components are the logic circuit and the load driven circuit. The logic circuit consists of four NMOS transistors with complementary pass logic and the load driven circuit consist of a combination of PMOS and NMOS transistors. This logic family is 3 to 9 times better than the static

CMOS logic regarding the power consumption aspect and approximately 3 times better than the 2N-2N2P [9].

The partial adiabatic logic circuits are ones that partially recover the charge and have the potential to perform robustly. The efficient charge recovery logic (ECRL) proposed by Moon et al [10] describes the cross coupled PMOS transistors and two NMOS transistors for the adiabatic logic. The disadvantage of this family is the coupling effect, as the two outputs are connected by a latch and being opposite to each other, they can interfere with each other.

The 2N-2N2P logic family is derived from the ECRL to reduce the coupling effect. The advantage of 2N-2N2P is that the cross coupled NMOS transistors result in non-floating outputs. Later a concept of positive feedback was introduced in the adiabatic logic families the positive feedback providednoise immunity and helped in the energy recovery process [11]. The energy consumption of this gate is lower than any other logic circuit of the same family. The integral part of the circuit is the latch made by two PMOS and NMOS transistors that prevent output degradation. This is a dual-rail circuit that generates both positive and negative outputs. The recent improvement in the adiabatic family by Kumar et.al

[12] proposed an EE-SPFAL which is a modified version of PFAL, EESPFAL aims to solve the information leakages issue encountered in PFAL by equalizing the load voltage before the next cycle commences. The output was refreshed before the next evaluation.

Proposed Approach

In this paper, we propose four adiabatic gates. AND/NAND and OR/NOR are implemented using both CPAL and PFAL methods respectively. Power for the gates is transmitted wirelessly followed by sine to square wave converter. The wave conversion is necessary for the adiabatic gates to work efficiently on square waves [12]. Subsequent subsections will give working of the proposed gates.

A. Wireless power clock

The power clock is mainly classified into four phases: Wait Phase, Evaluation Phase, Hold Phase and Recovery Phase. In the wait phase, the power clock is at a low state and typically waits for the inputs. During the evaluation phase voltage rises gradually from low to high. In this phase, the output is estimated based upon the inputs. The power clock remains in the high state in the hold phase. In the recovery phase power clock goes from high to low state. Note that the frequency of the power clock must be sufficiently higher than the inputs for distinguishable outputs.

B. Sine to square converter

The mentioned sine to square converter uses IC 714 along with some resistors. The voltage swing of the output square wave is dependent on the negative and positive power supply given to the IC 714. In this circuit a threshold voltage value is set to 0V. Whenever input crosses the threshold voltage output swings from one extreme to another extreme voltage. Thus, we get a square waveform which is obtained from the sine wave.

C. CPAL

The circuit diagram for CPAL AND gate is shown in Fig8. The circuit can be mainly divided into 3 parts: wireless transmission, sine to square wave conversion, CPAL logic. CPAL logic is further divided into a load-driven circuit and a logic function circuit. N1, N2, P1 and P2 form the load-driven part while N5-N8 are the components of the logic-driven part of the circuit [13]. The load-driven part is mainly responsible for energy saving while the logic function defines the operation of the gate. Transistors N3, N4 helps in grounding the load- driven transistors so that residual charge does not interfere with the next clock cycle [14].

D. PFAL

PFAL works in a similar fashion as CPAL. Here load driven part remains the same as CPAL. The logic function part differs in terms of transistor positioning. The power clock and sine to square wave conversion is unchanged.

Experimental Results

Fig 7 represents the simulation result of wireless CPAL OR/NOR gate. The inputs fed is square-wave with a peak voltage of 2V. Fig 8 represents the simulation result of wireless CPAL AND/NAND gate. The inputs fed is square-wave with a peak voltage of 2V. Fig 9 represents the simulation result of the wireless PFAL OR/NOR gate. The inputs fed square-wave with a peak voltage of 2V. Fig 9 represents the simulationresult of wireless PFAL AND/NAND gate. The inputs fed issquare-wave with a peak voltage of 2V. The power clock isoperating at 700KHz to generate a square wave with a peakvoltage of 4.8V for all the simulations. The smaller spikesobserved in the diagram are due to change in the phase of thepower clock. The power consumption of the proposed circuitTable I is compatible with similar power consumption as theexisting circuits.

TABLEI

Transistor count and power analysis experimental results of proposed wireless PFAL and CPAL logic gate circuits.

		CPAL	PFAL
Transistor count per gate	AND	10	8
	OR	10	8
Output current	AND	1.8653mA	3.902μA
	OR	1.8649mA	15.883μA
Power Dissipation		2.6395mW	1.7685mW

Conclusion

The PFAL and CPAL circuit described in this paper are dual-rail logic supplied by a wireless single-phase power clock. These circuits focus on the wireless charging and discharging of the load capacitors by switching the transistors in ON and OFF stats. This paper has presented a workingsimulation of wirelessly powered adiabatic logic circuits. The future work of this paper involves designing a 2:1 Mux using the proposed idea, inserting a CMOS hardware trojan circuit and detecting it using the power analysis method.

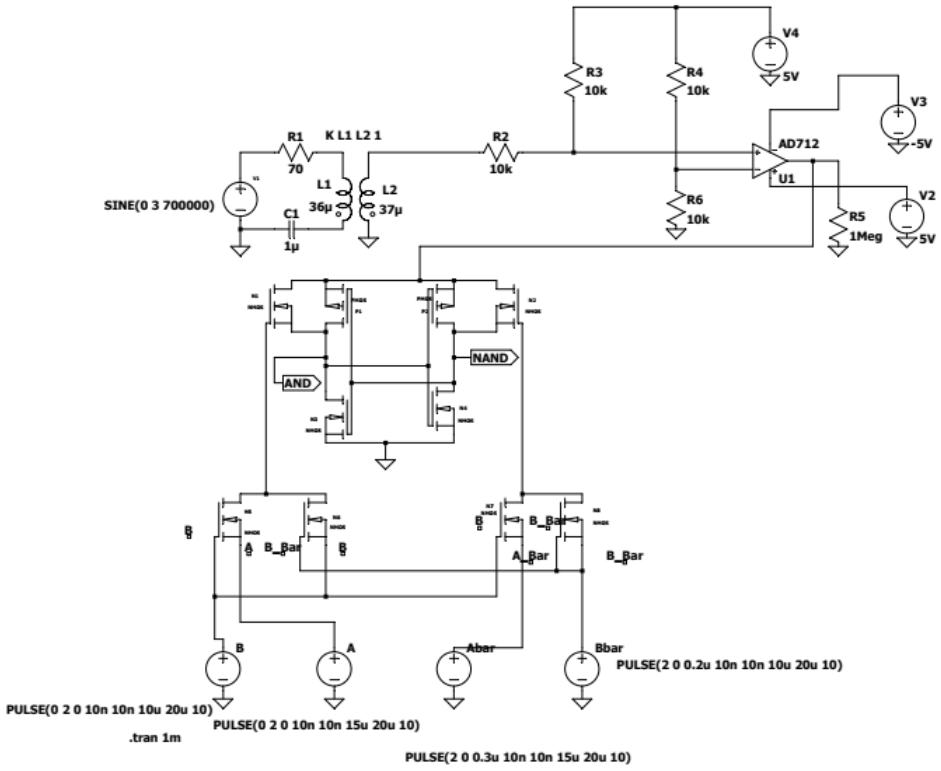

Fig. 3. Circuit diagram for CPAL AND gate.

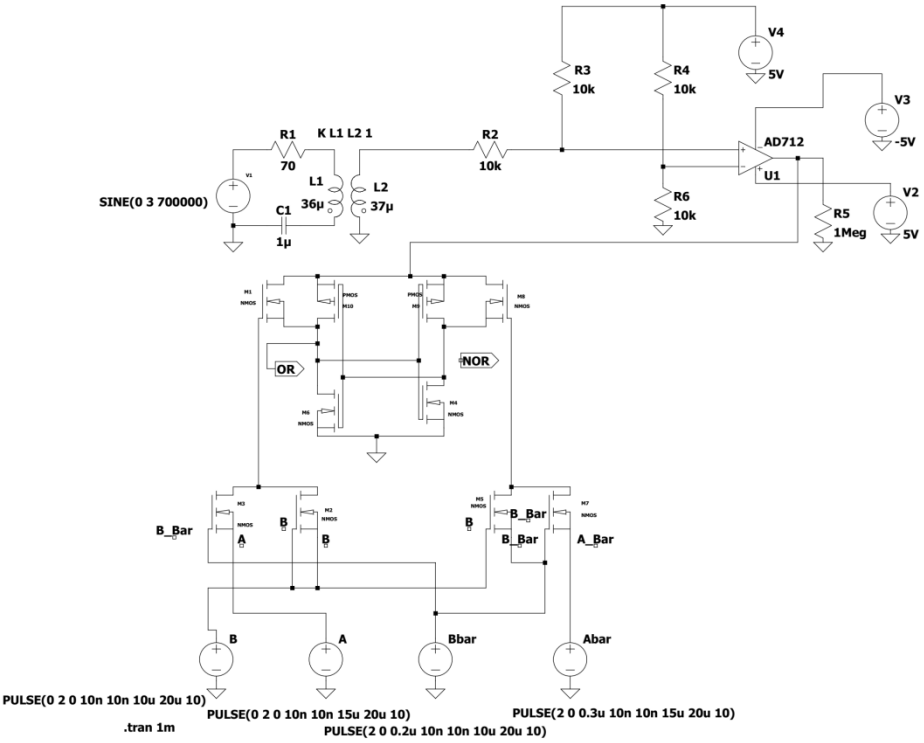

Fig. 4. Circuit diagram for CPAL OR gate.

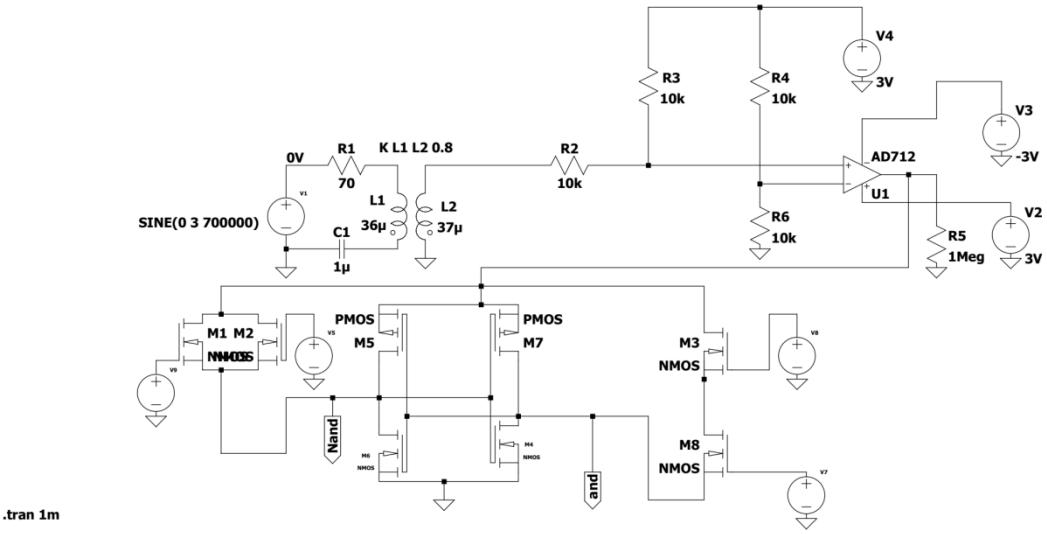

Fig. 5. Circuit diagram for PFAL AND gate.

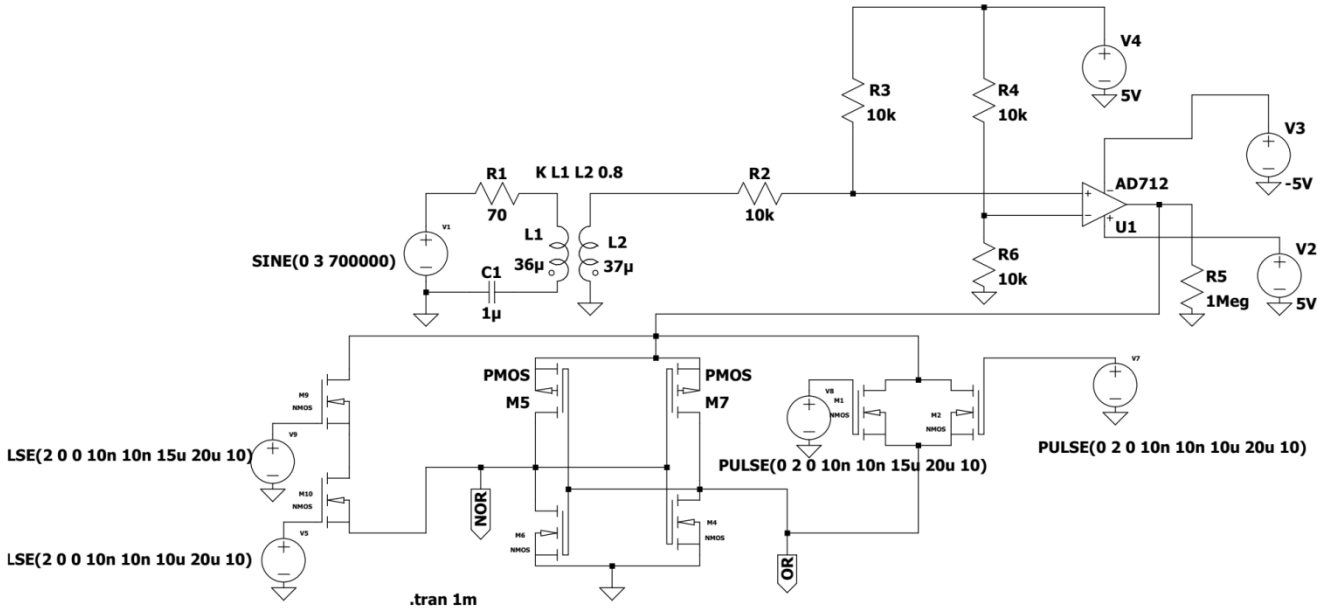

Fig. 6. Circuit diagram for PFAL OR gate.

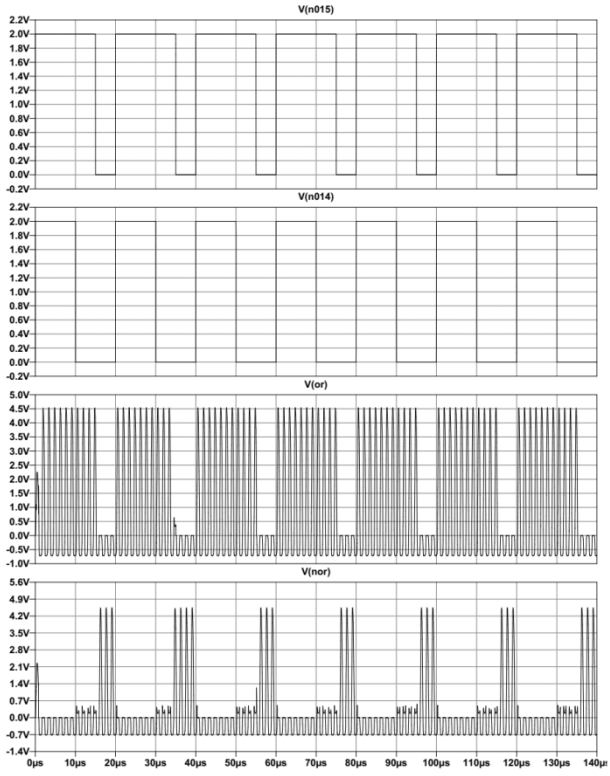

Fig. 7.Simulation results of CPAL OR gate, depicting two inputs, OR outputand NOR output

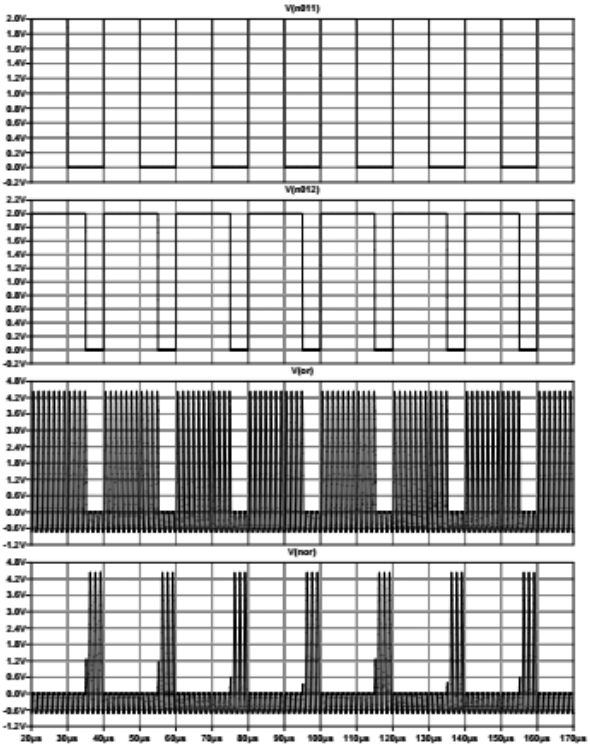

Fig. 8.Simulation results for CPAL AND gate, depicting two inputs, ANDoutput and NAND output

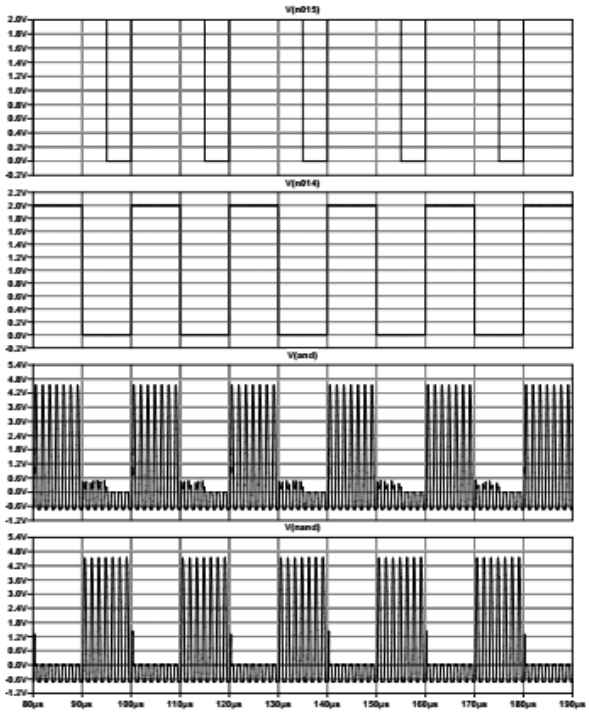

Fig. 9.Simulation results of PFAL OR gate, depicting two inputs, OR outputand NOR output.

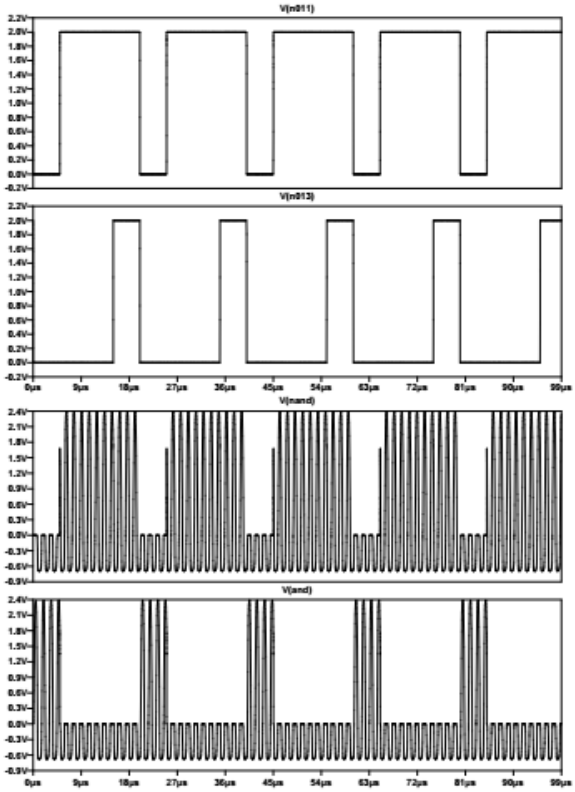

Fig. 10.Simulation results of PFAL ANDgate, depicting two inputs, ANDoutput and NAND output.

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